REMARKS

1. The application was filed with 23 claims. Claims 1-14 and 17-19 are pending in the application. Claims 15 and 16 have been cancelled. Amendments have been made to Claims 1, 4, 7, and 17. No new matter was entered in making the amendments. Applicant thanks the Examiner for withdrawing previous rejections under 35 U.S.C. § 103(a). The Examiner has rejected Claims 1-14 and 16-19 in the present Office Action.

2. In a telephonic interview on July 29, 2003, the undersigned and Examiner Cox discussed the rejections and the art cited against the present claims. The undersigned argued that the art cited was non-analogous and that the references did not describe or suggest all the limitations of the claimed inventions. The discussion centered on Claims 1 and 4. Examiner Cox mentioned that a clarification of the claim preambles to "consisting of," to limit the claims to four transistors might be helpful in clarifying the invention. The undersigned suggested clarifying the claims as "four-transistor" delay units. Agreement was not reached in any of the claims.

The present invention, we believe, is patentably distinct from the references cited because it has a different structure and performs in a different manner from the references. The differential controlled delay unit claimed in Claims 1 and 4 works by forcing both outputs of the delay stage to have 180° phase difference. With this design, the delay unit, also a two-stage amplifier, is able to use nearly all the voltage that is available between the positive and negative voltage rails. In other words, this four-transistor delay stage/amplifier uses substantially all the available voltage "headroom". This allows embodiments of the invention to have a larger range, in terms of voltage and of delay times, than it otherwise would have, if the claimed circuit had additional components, such as the extra switches shown in the Du and Proebsting references. This range advantage has been recognized. The claimed delay units of the present invention are both patentably different and much better than circuits in the prior art.

3. The Examiner has rejected claims 1-14 and 16-19 under 35 U.S.C. § 102(b) as being anticipated by U.S. Pat. No. 5,638,030 to He Du ("Du"). The Examiner states that Du discloses in Fig. 15 a circuit that essentially comprises the invention disclosed in Claims 1-14 and 16-19 of the present application, in that Du discloses a differential controlled delay unit comprising two amplifiers and four transistors.

Fig. 15 of Du does not disclose or suggest the claimed invention. As discussed below with respect to Proebsting and Mizuno, Du discloses a circuit seemingly similar to the inventions claimed in Claims 1-14 and 16-19. However, Du also includes other elements essential to the functioning of the circuit of Fig. 15, which make Du's circuits quite different from the claimed inventions. Fig. 15 of Du teaches an amplifier with a clipper transistor 4950 that greatly increases the frequency response of the circuit. Col. 8, lines 57-66. The clipper transistor provides a short that limits the output voltage of the delay circuit of which the clipper transistor is part. Thus, as stated in Du's background, "by limiting the voltage swing at its output nodes, rather than allowing it to swing rail to rail as in prior art differential amplifiers, the frequency response of the differential amplifier is much improved over such prior art differential amplifiers." Col. 1, lines 22-26. In other words, Du's circuits work faster (increased frequency response) because the clipper transistor limits the amplifiers to a shorter range of output voltages.

Thus, Du describes a circuit which functions in a manner opposite from the claimed invention, with a different and opposed goal: Du seeks to limit the voltage swings of the amplifiers for a better frequency response, while embodiments of the present invention seek to use the entire voltage range or "headroom" available. See present specification, p. 6, lines 1-4. In addition, Du requires elements that are not present in the claims, including the "clipper" transistor and its voltage source. Thus, Du does not describe a four-transistor differential controlled delay unit.

Nevertheless, in order to expedite prosecution, and without significantly narrowing the claims, Applicant has amended Claims 1 and 4 to recite that the controlled delay units with four transistors are "four transistor controlled delay" units in which "the delay unit uses substantially all available power supply voltage." Applicants request that the Examiner withdraw the rejection in view of the arguments above and the clarifying language of the amendment.

4. The Examiner has rejected claims 1, 4 and 6 under 35 U.S.C. § 102(e) as being anticipated by U.S. Pat. No. 6,164,064 to Robert Proebsting ("Proebsting"). Applicant traverses the rejection on grounds similar to those discussed above for Du. Fig. 1 of Proebsting has two portions, element 60 on the left side, to which the Examiner refers, and element 70 on the right side of Fig. 1. The text of Proebsting itself teaches against the use of the sense amplifier circuit 60 depicted in Fig. 1, stating that the "sense amplifier often does not generate output voltage signals capable of reaching the limits of a positive and negative voltage supply," and that requires the use of an additional amplifier 70. Col. 1, line 66, to col. 2, line 11. Thus, Proebsting does not describe or suggest a four or five transistor circuit, but a ten transistor circuit.

Even if we limit the discussion to only one half of the Proebsting circuit, the discussion above concerning voltage ranges and an extra transistor applies. Proebsting states, "This amplifier preferably requires a voltage supply exceeding a sum consisting of three transistor threshold voltages plus the differential voltage generated at the output terminals of the amplifier." Col. 1, lines 54-58 (emphasis added). In contrast, the present disclosure teaches a circuit in which no voltage "headroom" is wasted, as described above in the discussion of Du. In the present application, and as claimed in 1, there is no "switch" transistor requiring extra voltage from the power supply, and the claimed circuit uses nearly all the available positive input voltage. Application, p. 6, lines 1-4 ("the delay unit is able to use nearly all of the available positive input voltage"). Embodiments of the present invention, then, include an amplifier circuit without the "switch" transistor as shown in Proebsting.

The present office action states that the argument with respect to the elimination of element 28 in Fig. 1 has been considered, but is not persuasive. The argument, states the office action, is not persuasive because "there is no language in the claims that would exclude the delay unit from having additional elements." As also discussed above with Du, one substantial advantage of the present invention is the elimination of elements, such as element 28, from an amplifier circuit. Proebsting himself teaches against the use of only circuit 60 because it requires excessive voltage. A prior art reference must be considered in its entirety, including portions that teach away from the claims. M.P.E.P. 2141.02 at 2100-122. Proebsting does not anticipate the claimed

invention because the circuit disclosed in Proebsting is different from the claimed circuit, and Proebsting admits that the circuit functions in a manner different from the inventions claimed in Claims 1, 4, and 6.

Therefore, Proebsting does not anticipate the claimed invention, and the Examiner is requested to withdraw the rejections of Claims 1, 4 and 6 under 35 U.S.C. § 102(e). In any event, Proebsting does not teach a four-transistor controlled delay unit, but rather a 10-transistor two-stage amplifier in two parts. Nevertheless, in order to expedite prosecution, and without significantly narrowing the claims, Applicant has amended Claims 1 and 4 to recite that the controlled delay units with four transistors are "four transistor controlled delay" units in which "the delay unit uses substantially all available power supply voltage."

Applicants request that the Examiner withdraw the rejection in view of the arguments above and the clarifying language of the amendment. Applicants request that the Examiner withdraw the rejection over Proebsting because Proebsting does not describe or suggest the claimed invention, before or after the amendment.

5. The Examiner has rejected Claims 1-4 under 35 U.S.C. § 102(e) as being unpatentable over U.S. Pat. No. 6,414,556 to Masayuki Mizuno ("Mizuno"). The rejection states that Fig. 4 of Mizuno substantially discloses the circuit described by Claim 1 of the present application, as well as Claims 2 and 3. While the rejection includes Claim 4, no rejection is articulated with respect to Claim 4.

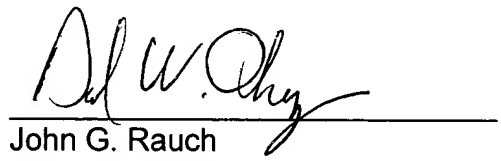
Applicants traverse the rejection. Mizuno is not directed to a delay unit, but to a level converter, as the rejection refers to in Fig. 4 of Mizuno. Fig. 4 does not describe or suggest a delay unit, but a six-transistor level converter, which is also depicted in Figs. 6 and 8 of Mizuno. In addition, the voltage converter of Fig. 4 does not have "a drain of the third and fourth transistors connected to a drain of the first and second transistors to form output terminals," as claimed in Claim 1 and Claim 4.

Therefore, the reference does not describe or suggest all the limitations of the inventions claimed in Claims 1 and 4 and in claims depending from them, Claims 2-3. The Examiner is respectfully requested to withdraw the rejections of Claims 1-4 under 35 U.S.C. § 102(e).

6. Applicant again thanks the Examiner for withdrawing previous rejections under 35 U.S.C. § 103(a). Applicant has amended the claims to clarify the components in the claimed four-transistor delay units. The amendments are not narrowing amendments in the sense of *Festo* because they clarify what is already claimed, a four-transistor delay unit that uses an available power supply voltage. *Festo Corporation v. Shoketsu Kinzoku Kogyo Kabushiki Co., Ltd*, 234 F.3d 558, 56 USPQ2d 1865 (Fed. Cir. 2000) (*en banc*), *overruled in part*, 535 U.S. 722, 62 U.S.P.Q.2d 1705 (2002). The amendment in Claim 7 corrects a grammatical error.

Applicant respectfully requests the Examiner to withdraw the rejections and to advance the Application to allowance.

Respectfully submitted,



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